National Semiconductor

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DP84322 Dynamic RAM Controller Interface Circuit for the 68000 CPU

General Description

The DP84322 dynamic RAM controller interface is a Programmable Array Logic (PAL®) device which allows for easy interface between the DP8409A, 17, 18, 19, 28, 29 dynamic RAM Controllers and the 68000/008/010 microprocessors.

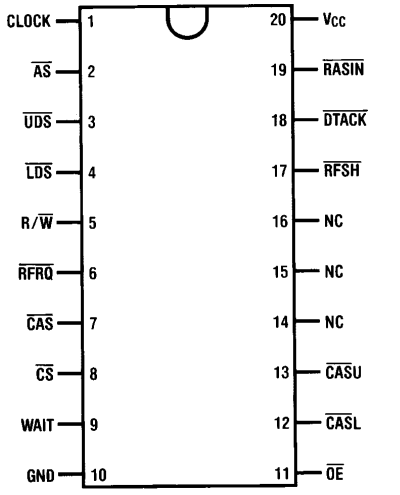
The DP84322 supplies all the control signals needed to perform memory read, write and refresh. Logic is included for inserting a wait state when using fast CPUs.

Features

- Provides 3-chip solution for the 68000 CPU and dynamic RAM interface (DP84300, DP84322, & DP8409A)
- Works with all 68000 speed versions
- Possibility of operation at 8 MHz with no wait states
- Performs hidden refresh
- $\overline{\text{DTACK}}$ is automatically inserted for both memory access and memory refresh
- Performs forced refresh using typically 4 CPU clocks
- Standard National Semiconductor PAL part (DMPAL16R4)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PAL in the National Semiconductor PAL family, including the new high speed PALs.

Connection and Block Diagrams

Dual-In-Line Package



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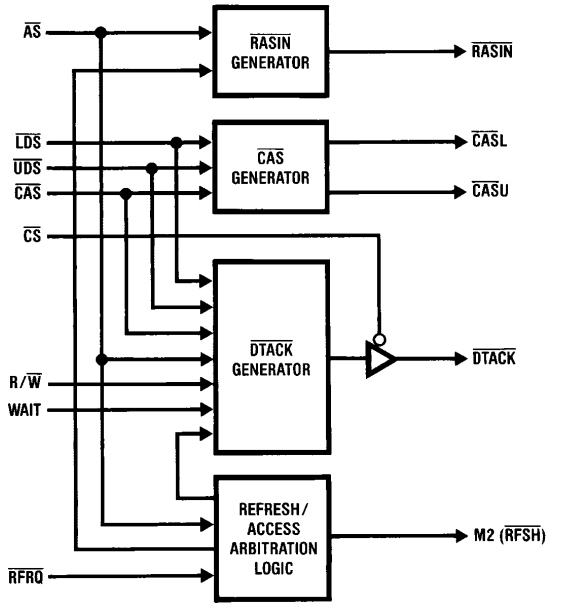
Top View

Order Number DP84322J or DP84322N
See NS Package Number J20A or N20A



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Recommended Operating Conditions (Commercial)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA

	Min	Typ	Max	Units
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225(1)	mA

Switching Characteristics over recommended ranges of temperature and V_{CC} (Note 3)

Symbol	Parameter		Test Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%			Units
				Min	Typ	Max	
t_{PD}	Input to Output		C_L = 50 pF		15	25	ns
t_{PD}	Clock to Output				10	15	ns
t_{PZX}	Pin 11 to Output Enable				10	20	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable		C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		13	25	ns
t_w	Width of Clock	High		15			ns
		Low		15			ns
t_{su}	Set-Up Time			25			ns
t_h	Hold Time			0	−10		ns

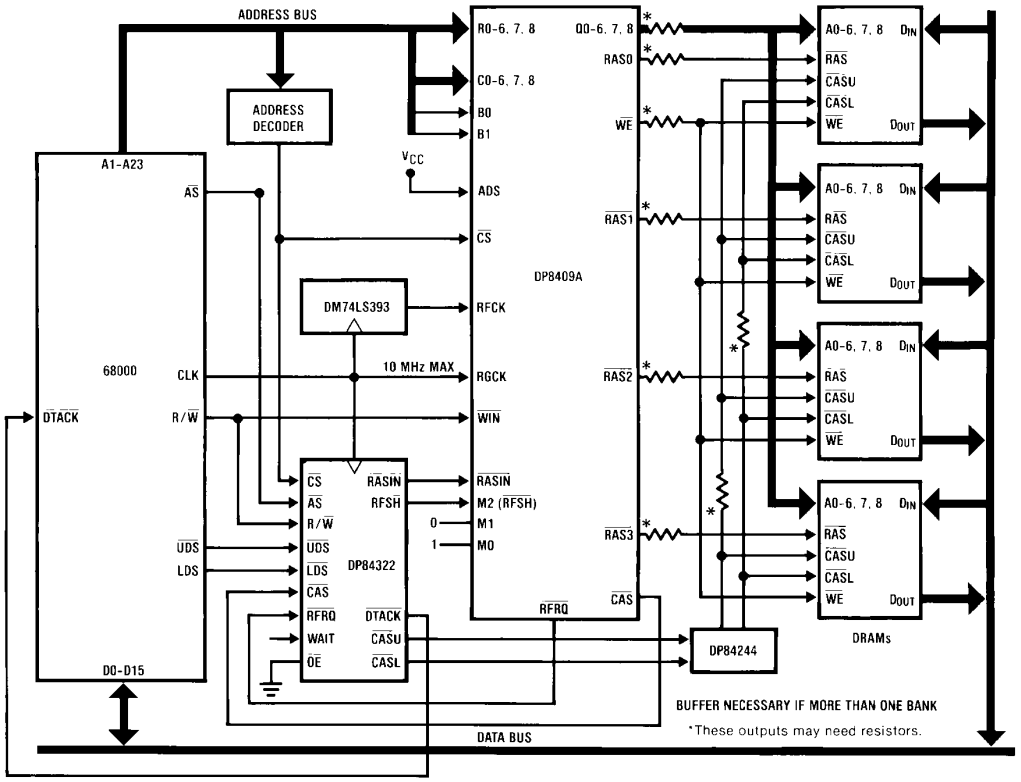
Note 1: I_{CC} = max at minimum temperature.

Note 2: One output at a time; otherwise 16 mA.

Note 3: If a PAL16R4B PAL is used, the Switching Characteristics will improve correspondingly.

System Block Diagram

DP84322 and DP8409A for 68000 CPU



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Mnemonic Description

INPUT SIGNALS

CLOCK — The clock signal determines the timing of the outputs and should be connected directly to the 68000 clock input.

$\overline{AS}$ — Address Strobe from the 68000 CPU. This input is used to generate $\overline{RASIN}$ to the DP8409A.

$\overline{UDS}$, $\overline{LDS}$ — Upper and lower data strobe from the 68000 CPU. These inputs, together with $\overline{AS}$, R/$\overline{W}$, provide $\overline{DTACK}$ to the 68000.

R/$\overline{W}$ — Read/write from the 68000 CPU, when WAIT = 0. Selects processor speed when WAIT = 1 (“1” = 4 to 6 MHz, “0” = 8 MHz).

$\overline{CAS}$ — Column Address Strobe from the DP8409A. This input, together with $\overline{LDS}$ and $\overline{UDS}$, provides two separate $\overline{CAS}$ outputs for accessing upper and lower memory data bytes.

$\overline{CS}$ — Chip Select. This input enables $\overline{DTACK}$ output. $\overline{CS}$ = 0, $\overline{DTACK}$ output is enabled; $\overline{CS}$ = 1, $\overline{DTACK}$ output is TRI-STATE®.

$\overline{RFRQ}$ — Refresh Request. This input requests the DP84322 for a forced refresh.

WAIT — This input allows the necessary wait state to be inserted for memory access cycles.

OUTPUT SIGNALS

$\overline{RASIN}$ — This output provides a memory cycle start signal to the DP8409A and provides $\overline{RAS}$ timing during hidden refresh.

$\overline{CASU}$, $\overline{CASL}$ — These signals are the separate $\overline{CAS}$ outputs needed for byte writing.

$\overline{DTACK}$ — This output is used to insert wait states into the 68000 memory cycles when selected and during a forced refresh cycle where the CPU attempts to access the memory. This output is enabled when $\overline{CS}$ input is low and at TRI-STATE when $\overline{CS}$ is high.

$\overline{RFSH}$ — This output controls the mode of the DP8409A. It always goes low for 4 CPU clock periods when $\overline{AS}$ is inactive and a forced refresh is requested through $\overline{RFRQ}$ input. This allows the DP8409A to perform an automatic forced refresh.

Functional Description

MEMORY ACCESS

As a 68000 bus cycle begins, a valid address is output on the address bus A1–A23. This address is decoded to provide Chip Select ($\overline{CS}$) to the DP8409A. After the address becomes valid, $\overline{AS}$ goes low and it is used to set $\overline{RASIN}$ low from the DP84322 interface circuit. Note that $\overline{CS}$ must go low for a minimum of 10 ns before the assertion of $\overline{RASIN}$ for a proper memory access. As an example, with a 8 MHz 68000, the address is valid for at least 30 ns before $\overline{AS}$ goes active. $\overline{AS}$ then has to ripple through the DP84322 to produce $\overline{RASIN}$. This means the address is valid for a minimum of 40 ns before $\overline{RASIN}$ goes low, and the decoding of $\overline{CS}$ should take less than 30 ns. At this speed the DM74LS138 or DM74LS139 decoders can be selected to guarantee the 10 ns minimum required by $\overline{CS}$ set-up time going low before the access $\overline{RASIN}$ goes low (t_{CSRL} of the DP8409A). This is important because a false hidden refresh may take place when the minimum t_{CSRL} is not met. Typically $\overline{RASIN}$ occurs at the end of S2. Subsequently, selected $\overline{RAS}$ output, row to column select and then $\overline{CAS}$ will automatically follow $\overline{RASIN}$ as determined by mode 5 of the DP8409A. Mode 5 guarantees a 30 ns minimum for row address hold time (t_{RAH}) and a minimum of 8 ns column address set-up time (t_{ASC}). If the system requires instructions that use byte writing, then $\overline{CAS}$U and $\overline{CAS}$L are needed for accessing upper and lower memory data bytes, and they are provided by the DP84322. In the DP84322, $\overline{LDS}$ and $\overline{UDS}$ are gated with $\overline{CAS}$ from the DP8409A to provide $\overline{CAS}$L and $\overline{CAS}$U, therefore designers need not be concerned about delaying $\overline{CAS}$ during write cycles to assure valid data being written into memory. The 8 MHz 68000 specifies during a write cycle that data output is valid for a minimum of 30 ns before $\overline{DS}$ goes active. Thus, $\overline{CAS}$L and $\overline{CAS}$U will not go low for at least 40 ns after the output data becomes stable, guaranteeing the 68000 valid data is written to memory.

Furthermore, the gating of $\overline{UDS}$, $\overline{LDS}$ and $\overline{CAS}$ allows the DP84322 interface controller to support the test and set instruction (TAS). The 68000 utilizes the read-modify-write cycle to execute this instruction. The TAS instruction provides a method of communication between processors in a multiple processor system. Because of the nature of this instruction, in the 68000, this cycle is indivisible and the Address Strobe $\overline{AS}$ is asserted throughout the entire cycle, however $\overline{DS}$ is asserted twice for two accesses: a read then a write. The dynamic RAM controller and the DP84322 respond to this read-modity-write instruction as follows (refer to the TAS instruction timing diagram for clarification). First, the selected $\overline{RAS}$ goes low as a result of $\overline{AS}$ going low, and this $\overline{RAS}$ output will remain low throughout the entire cycle. Then the DP84322's selected $\overline{CAS}$ output ($\overline{CAS}$L or $\overline{CAS}$U) goes low to read the specified data byte. After this read, $\overline{DS}$ goes high causing the selected $\overline{CAS}$ to go high. A few clocks later R/$\overline{W}$ goes low and then $\overline{DS}$ is reasserted. As $\overline{DS}$ goes low, the selected $\overline{CAS}$ goes low strobing the CPU's modified data into memory, after which the cycle is ended when $\overline{AS}$ goes high.

The two $\overline{CAS}$ outputs from the DP84322, however, can only drive one memory bank. For additional driving capability, a memory driver such as the DP84244 should be added to drive loads of up to 500 pF.

Since this DP84322 interface circuit is designed to operate with all of the 68000 speed versions, a status input called WAIT is used to distinguish the 8 MHz from the others. The WAIT input should be set low for 6 MHz or less allowing full speed of operation with no wait states. Data Transfer Acknowledge input ($\overline{DTACK}$) of the 68000 at these speeds is automatically inserted during S2 for every memory transaction cycle and is then negated at the end of that cycle when $\overline{UDS}$ and/or $\overline{LDS}$ go high. For the 8 MHz 68000 however, a wait state is required for every memory transaction cycle. At these speeds, the WAIT input is set high, selecting the DP8409A's $\overline{CAS}$ output to generate $\overline{DTACK}$ and again $\overline{DTACK}$ is negated at the end of the cycle when $\overline{UDS}$ or $\overline{LDS}$ goes high. Note that $\overline{DTACK}$ output is enabled only when the DP8409A's $\overline{CS}$ is low. Therefore when the 68000 is accessing I/O or ROM (in other words, when the DP8409A is not selected), the DP84322's $\overline{DTACK}$ output goes high impedance logic '1' through the external pull-up resistor and it is now up to the designer to supply $\overline{DTACK}$ for a proper bus cycle.

The following table indicates the maximum memory speed in terms of the DRAM timing parameters: t_{CAC} (access-time from $\overline{CAS}$) and t_{RP} ($\overline{RAS}$ precharge time) required by different 68000 speed versions:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RP}	Minimum t_{RAS}
8 MHz	125 ns	140 ns	220 ns
6 MHz	90 ns	170 ns	290 ns
4 MHz	270 ns	280 ns	450 ns

Pin 5 (R/$\overline{W}$ input to the DP84322) is not used as R/$\overline{W}$ when the WAIT input is high. Therefore, when WAIT is high and pin 5 is low, this is configured for the 8 MHz 68000. The dynamic RAM controller in this configuration operates in mode 5 and mode 1.

When both WAIT and pin 5 are high, this is configured for 4 MHz and 6 MHz 68000, allowing only two microprocessor clocks for memory refresh. Furthermore, the designer can use the DP8408A because the dynamic RAM controller now operates in mode 0 and mode 5 or mode 6. In addition, the programmable refresh timer, DP84300, should be used to determine the refresh rate (RFCK) and to provide the refresh request ($\overline{RFRQ}$) input to the DP84322. The refresh timer can provide over two hundred different divisors. $\overline{RFRQ}$ is given at the beginning of every RFCK cycle and remains active until M2 goes low for memory refresh. The DP84322 samples $\overline{RFRQ}$ when $\overline{AS}$ is high, then sets M2 low for two microprocessor clocks, taking the DP8408A or DP8409A to the external control refresh mode. $\overline{RASIN}$ for this refresh is also issued by the DP84322. If a memory access is pending, $\overline{RASIN}$ for this access will not be given until it is delayed for approximately one microprocessor clock, allowing $\overline{RAS}$ precharge time for the dynamic RAMs.

The following table indicates different memory speeds in terms of the DRAM parameters required by 4 MHz and 6 MHz 68000:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RAS}	Minimum t_{RP}	Minimum t_{RAH}
4 MHz	290 ns	200 ns	225 ns	20 ns
6 MHz	110 ns	125 ns	140 ns	20 ns

DP8408A, DP8409A operate in mode 6 and mode 0.

Functional Description (Continued)

When WAIT = 1, pin 5 = 0 (8 MHz), the PAL controller supports read and write cycles with one inserted wait state, forced refresh with five wait states inserted if $\overline{CS}$ is valid, and hidden refresh. This PAL mode does not support the TAS instruction.

When WAIT = pin 5 = 1 (4–6 MHz), the PAL controller supports read and write cycles with no wait states inserted, and forced refresh with two wait states inserted if $\overline{CS}$ is valid. This PAL mode does not support the TAS instruction and only supports hidden refresh when used in mode 5 with the DP8409A controller.

The DP84322 can possibly be operated at 8 MHz with no wait states (WAIT = "0") given the following conditions:

FAST PAL (PAL16R4A)

S2 + S3 + S4 + S5 = 250 ns

$\overline{RASIN}$ delay = 60 ns ($\overline{AS}$ low max.)

+ 25 ns (Fast PAL delay) = 85 ns max.

$\overline{RASIN}$ to $\overline{CAS}$ delay DP8409-2 = 130 ns max.

External $\overline{CASH,L}$ generation using 74S02 and 74S240

7.5 ns (74S02) + 10 ns (74S240) − 7.5 ns (less load on 8409 $\overline{CAS}$ line) = 10 ns max.

Transceiver delay (74LS245) = 12 ns max.

68000 data setup into S6 = 40 ns min.

$\therefore$ Minimum t_{CAC} = 53 ns

= 250 − 85 − 130 − 10 − 12 + 40

Minimum t_{RAS} = 240 ns

Minimum t_{RP} = 150 ns

Minimum t_{RAH} = 20 ns

REFRESH CYCLE

Since the access sequence timing is automatically derived from $\overline{RASIN}$ in mode 5, R/$\overline{C}$ and $\overline{CASIN}$ are not used and now become Refresh Clock (RFCK) and $\overline{RAS}$-generator clock (RGCK) respectively. The Refresh Clock RFCK may be divided down from RGCK, which is the microprocessor clock, using the DM74LS393 or DM74LS390. RFCK provides the refresh time interval and RGCK the fast clock for all-$\overline{RAS}$ refresh if forced refreshing is necessary. The DP8409A offers both hidden refresh in mode 5 and forced refresh in mode 1 with priority placed on hidden refreshing. Assume 128 rows are to be refreshed, then a 16 μs maximum clock period is needed for RFCK to distribute refreshing of all the rows over the 2 ms period.

The DP8409A provides hidden refreshing in mode 5 when the refresh clock (RFCK) is high and the microprocessor is not accessing RAM. In other words, when the DP8409A's chip select is inactive because the microprocessor is accessing elsewhere, all four $\overline{RAS}$ outputs follow $\overline{RASIN}$, strobing the contents of the on-chip refresh counter to every memory bank. $\overline{RASIN}$ going high terminates the hidden refresh and also increments the refresh counter, preparing it for the next refresh cycle. Once a hidden refresh has taken place, a forced refresh will not be requested by the DP8409A for the current RFCK cycle.

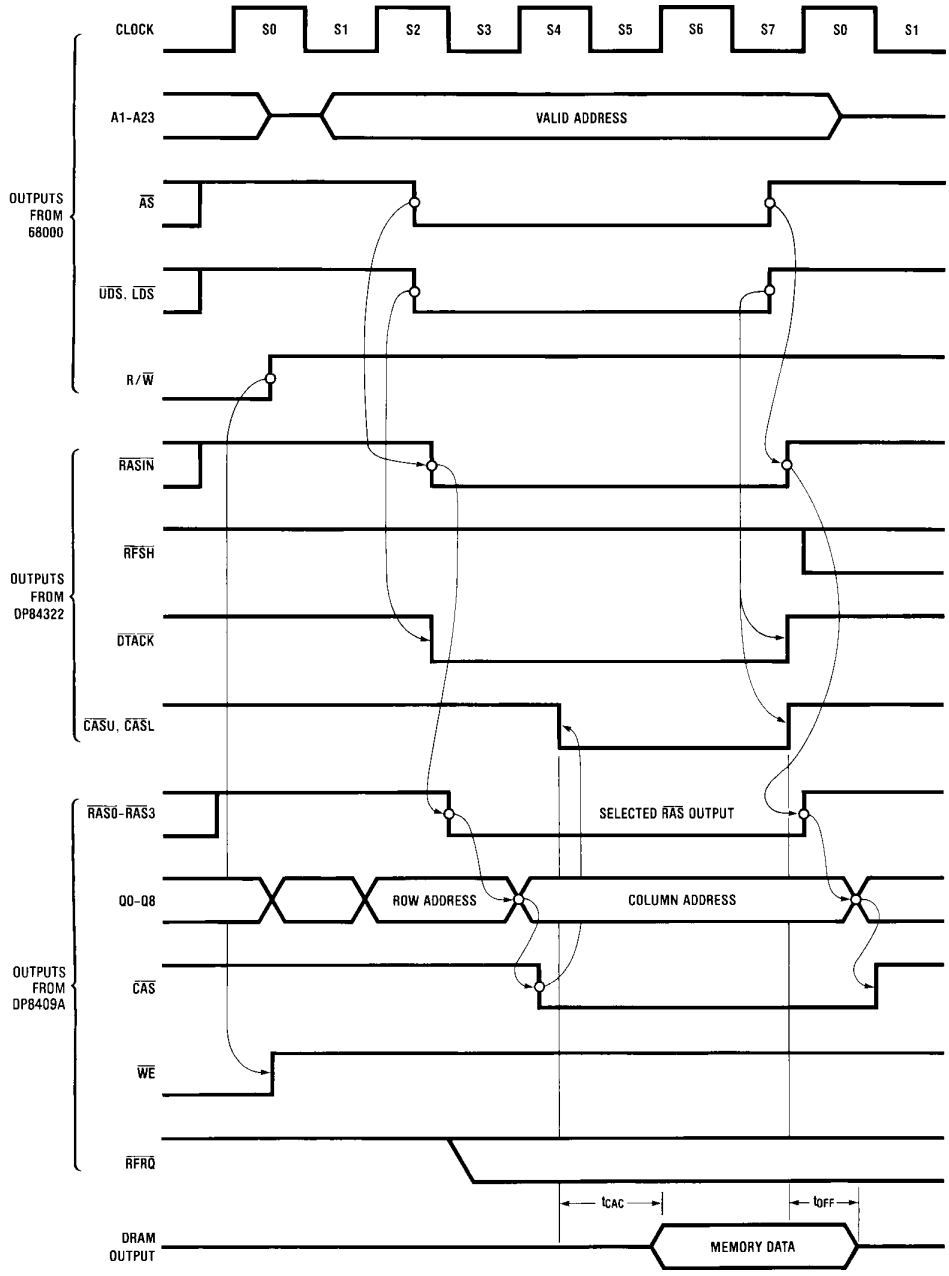
However, if the microprocessor continuously accessed the DP8409A and memory while RFCK was high, a hidden refresh could not have taken place and now the system must force a refresh. Immediately after RFCK goes low, the Refresh Request signal ($\overline{RFRQ}$) from the DP8409A goes low, indicating a forced refresh is necessary. First, when $\overline{RFRQ}$ goes low any time during S2 to S7, the controller interface circuit waits until the end of the current memory access cycle and then sets M2 ($\overline{RFSH}$) low. This refresh takes four microprocessor clocks to complete. If the current cycle is another memory cycle, the 68000 will automatically be put in four wait states. Alternately, when $\overline{RFRQ}$ goes low while $\overline{AS}$ is high during S0 to S1, M2 is now set low at S2. Therefore, it requires an additional microprocessor clock for this refresh. Once the DP8409A is in mode 1 forced refresh, all the $\overline{RAS}$ outputs remain high until two RGCK trailing edges after M2 goes low, when all $\overline{RAS}$ outputs go low. This allows a minimum of one and a half clock periods of RGCK for $\overline{RAS}$ precharge time. As specified in the DP8409A data sheet, the $\overline{RAS}$ outputs remain low for two clock periods of RGCK. The refresh counter is incremented as the $\overline{RAS}$ outputs go high. Once the forced refresh has ended, M2 is brought high, the DP8409A back to mode 5 auto access. Note that $\overline{RASIN}$ for the pending access is not given until it has been delayed for a full microprocessor clock, allowing $\overline{RAS}$ precharge time for the coming access.

If the 68000 bus is inactive (i.e., the 68000's instruction queue is full, or the 68000 is executing internal operations such as a multiply instruction, or the 68000 is in halt state . . .) and a refresh has been requested, a refresh will also take place because $\overline{RFRQ}$ is continuously sampled while $\overline{AS}$ is high. Therefore, refreshing under these conditions will be transparent to the microprocessor. Consequently, the system throughput is increased because the DP84322 allows refreshing while the 68000 bus is inactive.

The 84322 is a standard National Semiconductor PAL part (DMPAL16R4). The user can modify the PAL equations to support his particular application. The 84322 logic equations function table (functional test), and logic diagram can be seen at the end of this data sheet.

System Timing Diagrams

68000 Memory Read Cycle (Wait = 0, Pin 5 = R/$\overline{W}$)



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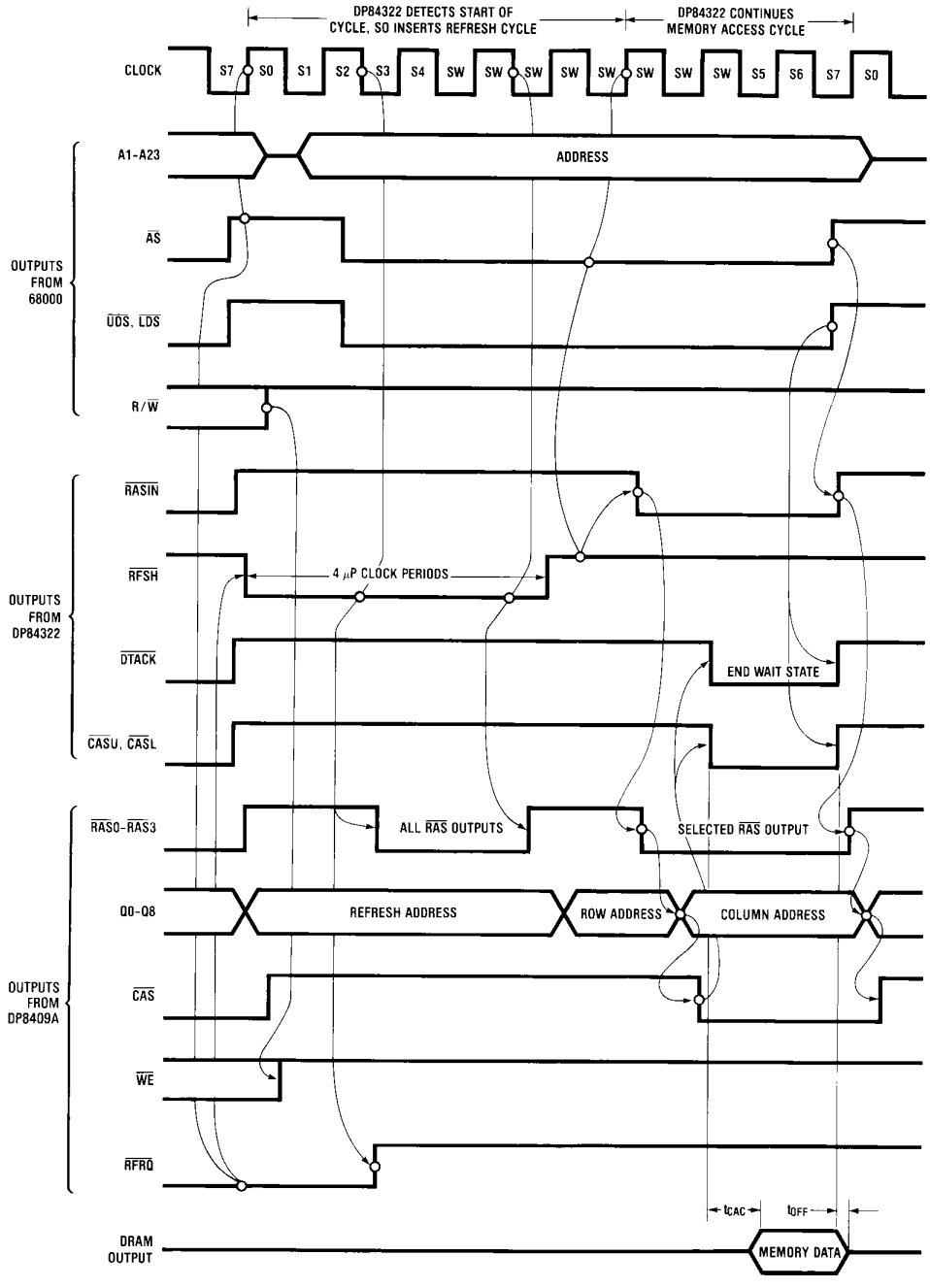
System Timing Diagrams (Continued)

68000 Memory Read Cycle and Forced Refresh (Wait = 0, Pin 5 = R/$\overline{W}$)
(4 Wait Clock Periods Inserted for Forced Refresh)



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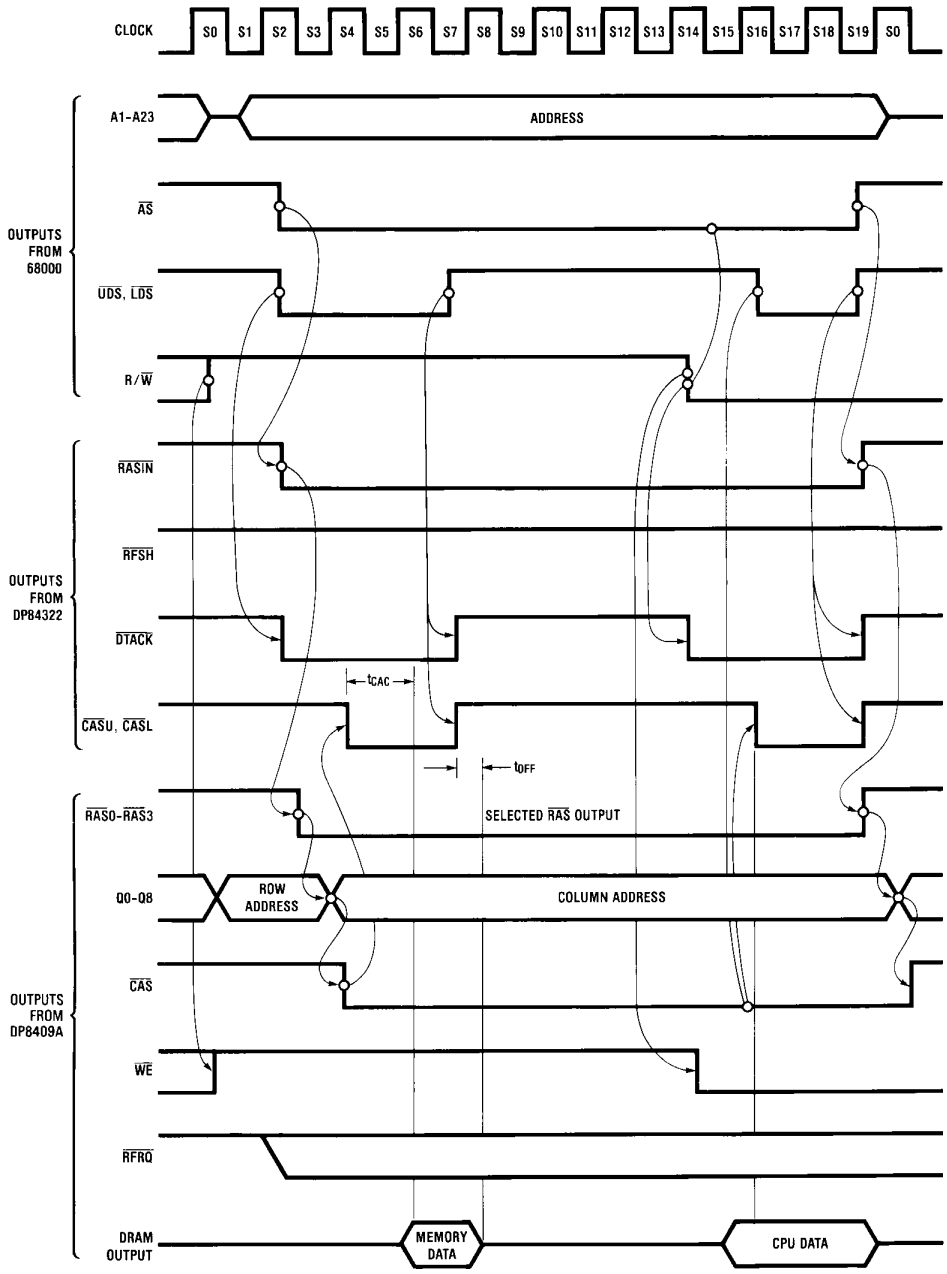
System Timing Diagrams (Continued)

TAS Instruction Cycle (Wait = 0, Pin 5 = R/$\overline{W}$)



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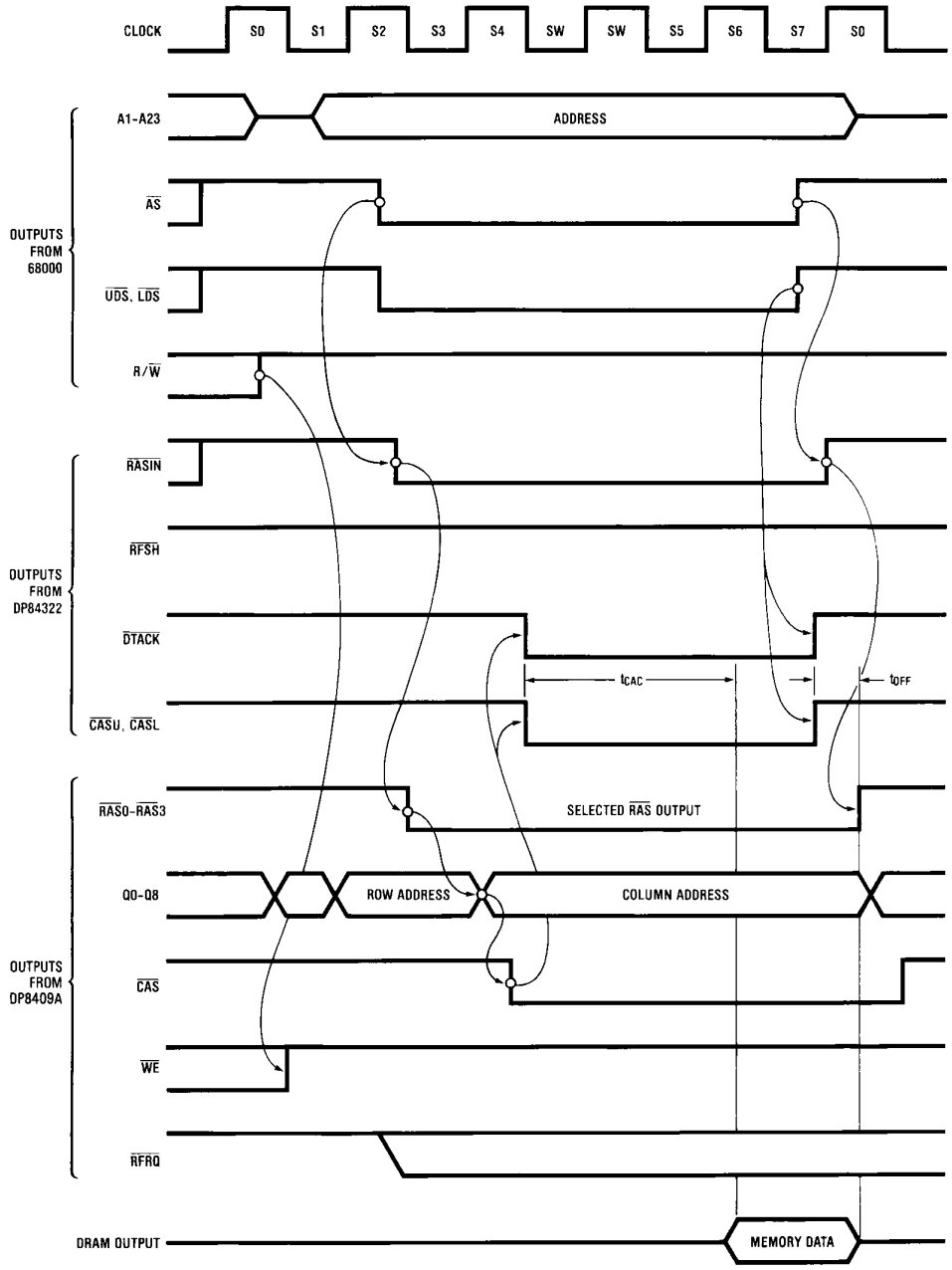
System Timing Diagrams (Continued)

Memory Read Cycle (Wait = 1, Pin 5 = 0)



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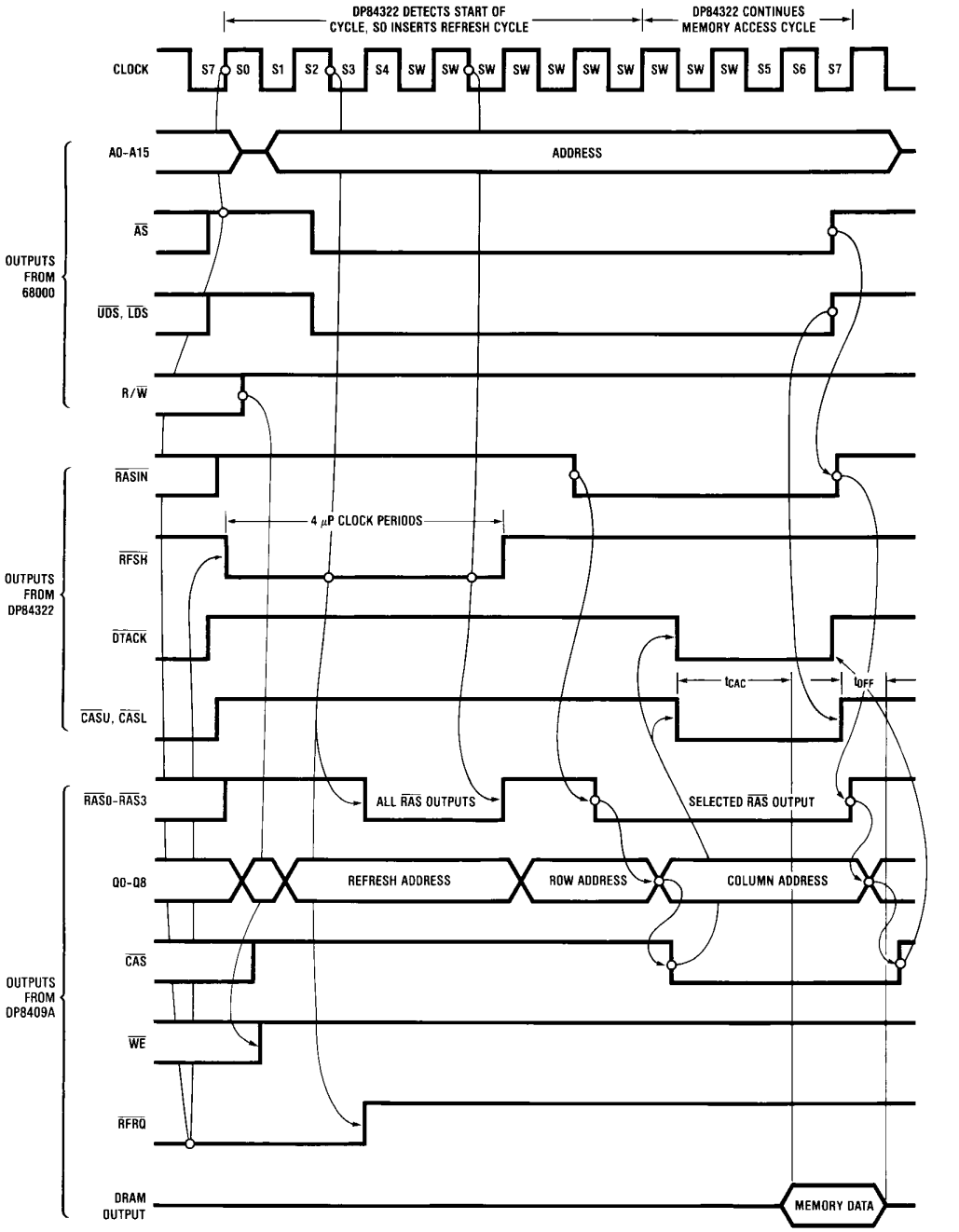
System Timing Diagrams (Continued)

Memory Read Cycle and Forced Refresh (Wait = 1, Pin 5 = 0)



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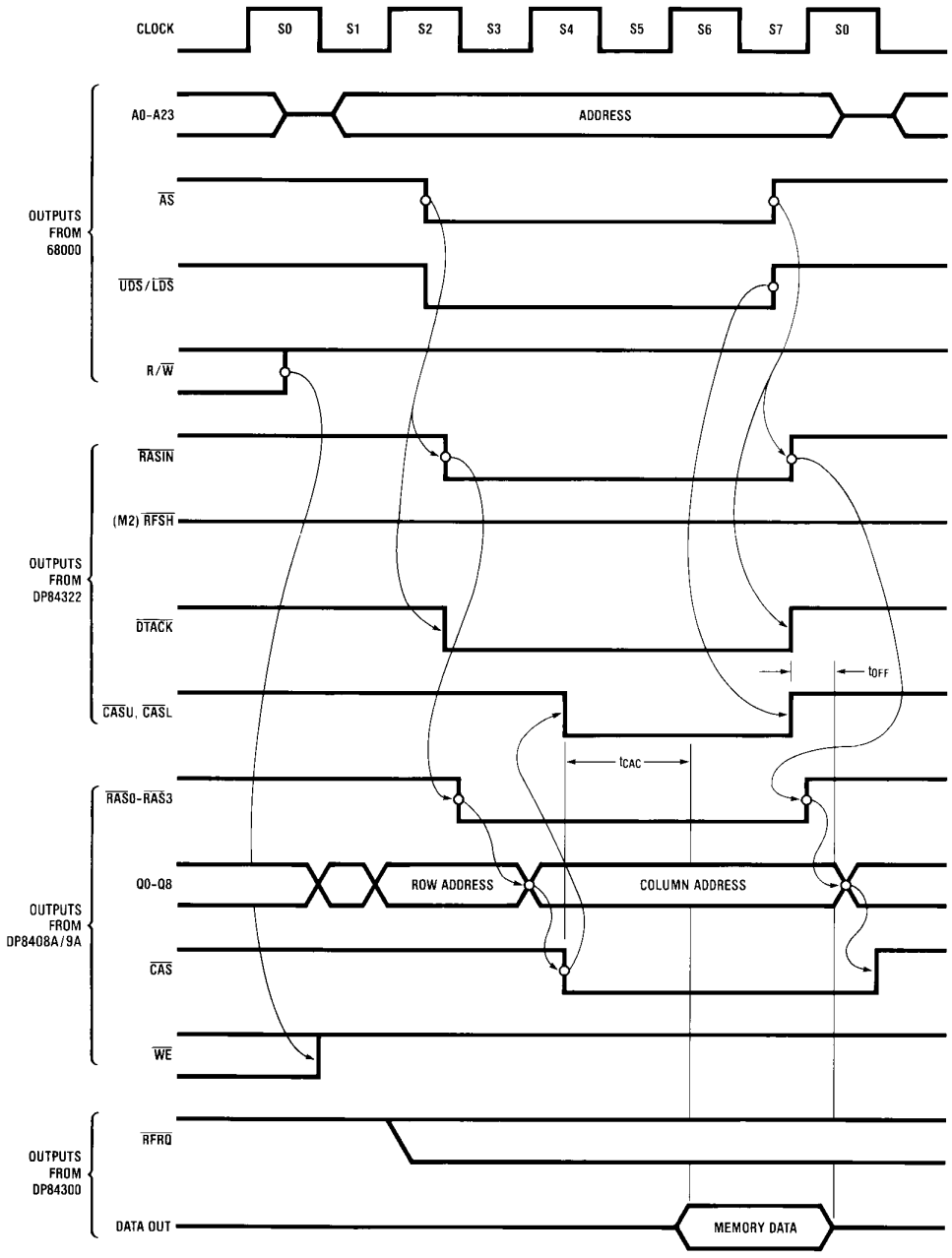
System Timing Diagrams (Continued)

68000 Memory Read Cycle (Wait and Pin 5 = 1)



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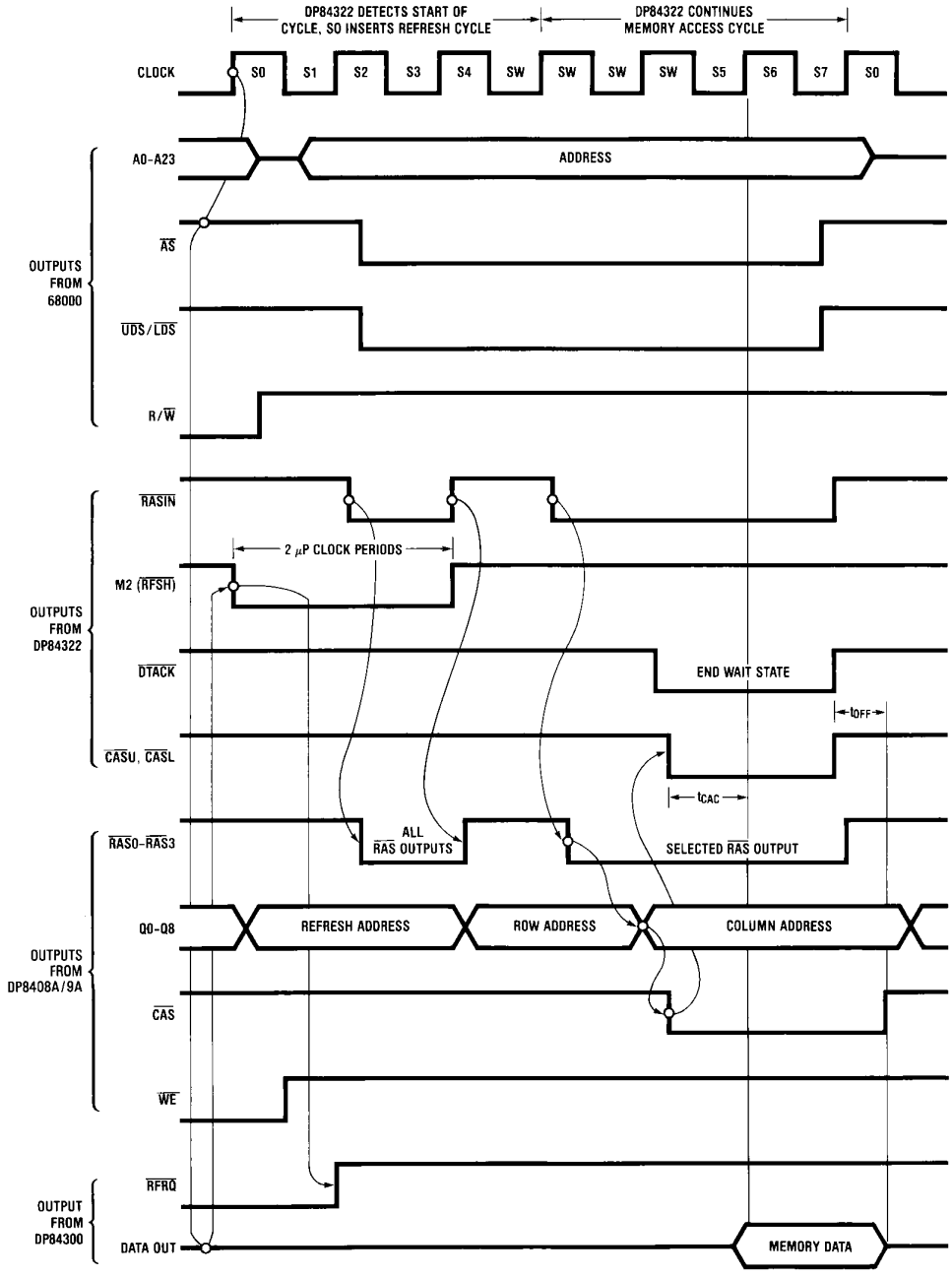
System Timing Diagrams (Continued)

68000 Memory Read Cycle and Memory Refresh (Wait and Pin 5 = 1)



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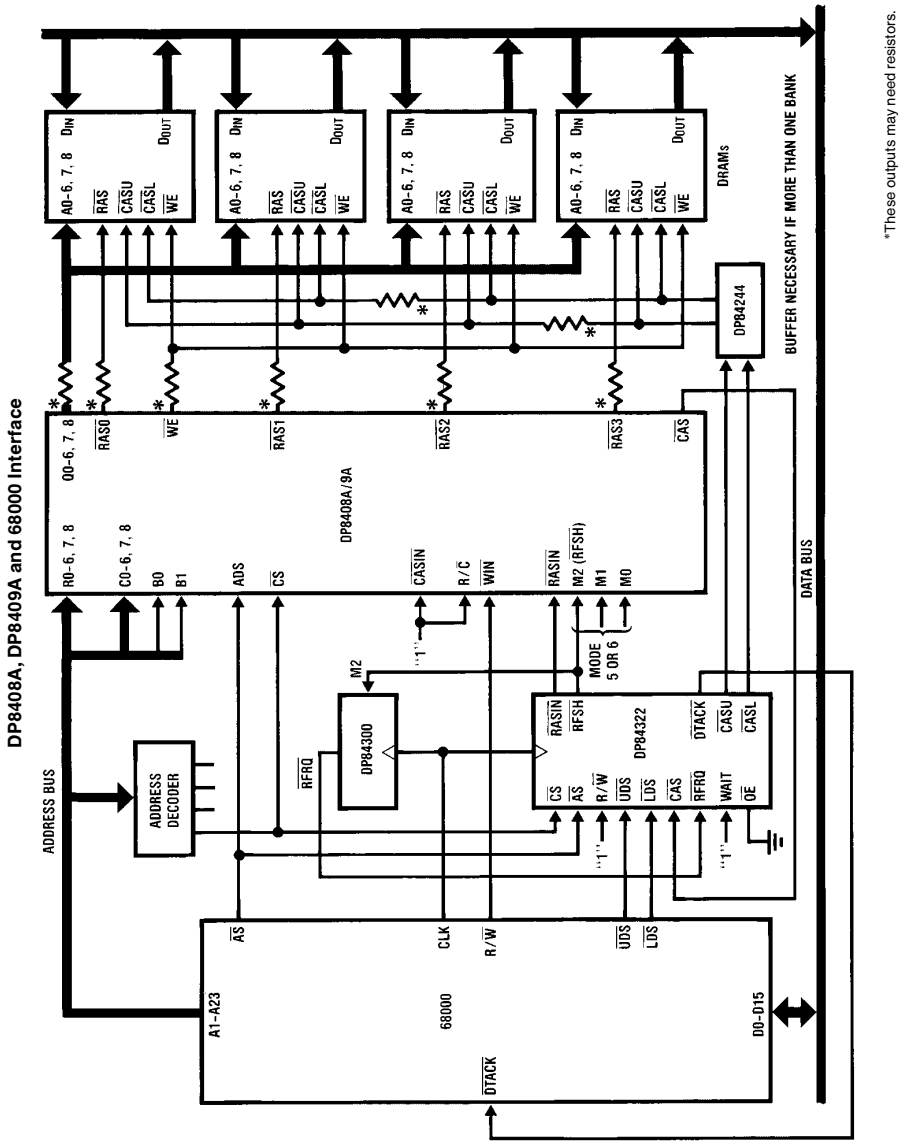
Modified System Block Diagram



PAL Boolean Equations

PAL16R4 DP84322 Dynamic RAM Controller Interface for the MC68000-DP8409A Memory System

CK /AS /UDS /LDS R /RFRQ /CAS /CS WAIT GND /OE /CL /CU /C /B /A /RFSH /DTACK /RASIN VCC

IF (VCC) RASIN = AS • /RFSH • /A + RFSH • R • A • WAIT

IF (CS) DTACK = /R • CAS • WAIT + UDS • /A • /B • /WAIT + LDS • /A • /B • /WAIT + AS • /R • /A • /B • /WAIT + AS • /RFSH • R • /A • /B • WAIT

RFSH: = /AS • RFRQ + RFSH • /R • /C • WAIT + RFSH • R • /A • WAIT + RFSH • /C • /WAIT

A: = RFSH

B: = A

C: = B

IF (VCC) CU = UDS • CDS

IF (VCC) CL = LDS • CAS

Function Table

CK	$\overline{AS}$	$\overline{UDS}$	$\overline{LDS}$	R	$\overline{RFRQ}$	$\overline{CAS}$	$\overline{CS}$	WAIT	$\overline{OE}$	$\overline{CL}$	$\overline{CU}$	$\overline{C}$	$\overline{B}$	$\overline{A}$	$\overline{RFSH}$	$\overline{DTACK}$	$\overline{RASIN}$
C	H	L	L	H	H	H	H	L	L	H	H	X	X	X	X	X	H
C	H	L	L	H	H	L	H	L	L	L	L	X	X	X	X	X	H
C	H	L	H	H	H	L	H	L	L	H	L	X	X	X	X	X	H
C	H	H	L	H	H	L	H	L	L	L	H	X	X	X	X	X	H
C	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	Z	H
C	L	L	H	H	H	H	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	H	H	L	L	L	L	H	L	H	H	H	H	L	L
C	L	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	L
C	L	H	H	L	H	L	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	L	H	L	L	L	L	H	L	H	H	H	H	L	L
C	H	H	H	L	H	H	L	L	L	H	H	H	H	H	H	H	H
C	H	H	H	L	L	H	L	L	L	H	H	H	H	H	L	H	H
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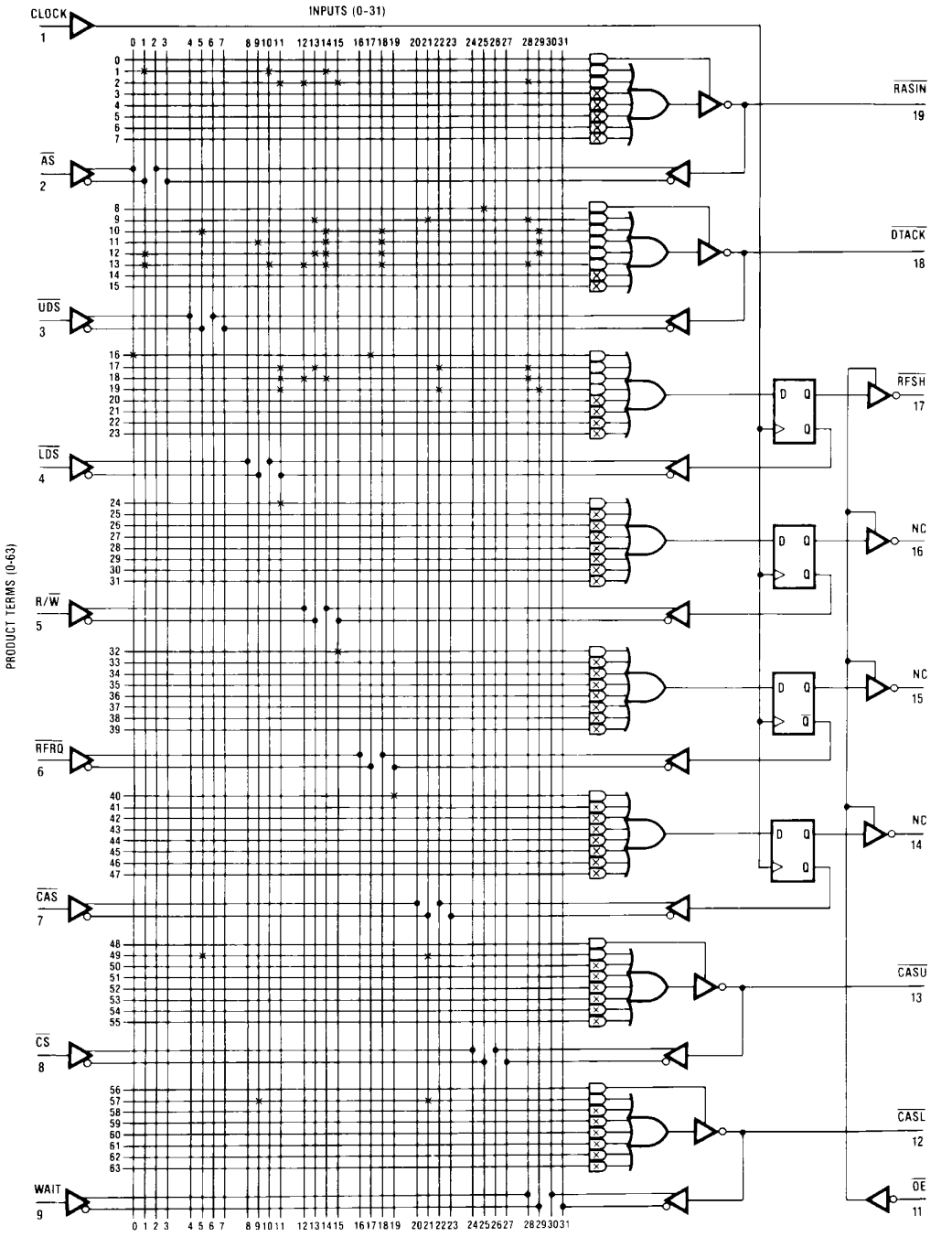
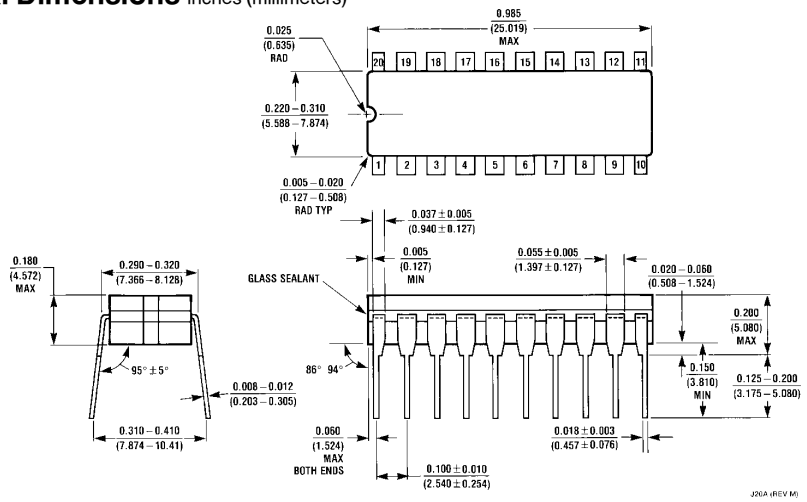
C	L	L	L	L	H	H	L	H	L	H	H	L	L	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	L	H	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	L	L	H	L	L	H	L	L	L	L	H	H	H	L	L
C	H	H	H	L	H	L	L	H	L	H	H	H	H	H	H	L	H
C	H	H	H	L	H	H	H	H	L	H	H	H	H	H	H	Z	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	L	L	H	L
C	L	L	H	H	H	H	L	H	L	H	H	H	L	L	H	H	H
C	L	L	H	H	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	H	H	H	L	L	H	L	H	L	L	H	H	H	L	L
C	H	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	H
C	H	H	H	H	H	H	L	H	H	H	H	Z	Z	Z	Z	H	H

DP84322 Logic Diagram PAL 16R4

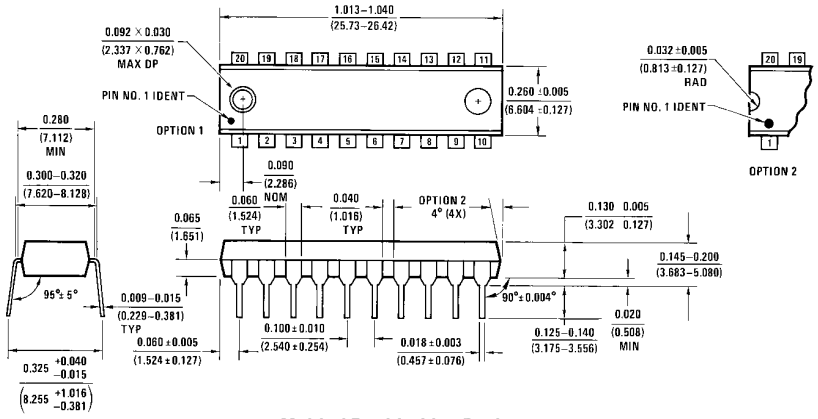


TL/F/5003–12

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package
Order Number DP84322J
NS Package Number J20A



Molded Dual-In-Line Package
Order Number DP84322N
NS Package Number N20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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